

13 floating gate and being separated from said floating gate by said second insulation layer, said
14 second portion having a surface substantially parallel to and opposing said first side wall;
15 an erase gate formed over a second one of said side walls and over at least a portion of
16 said top surface of said floating gate and being separated from said second one of said side walls
17 by said second insulation layer;
18 a drain region formed in a portion of said substrate proximate said control gate; and
19 a source region formed in a portion of said substrate proximate said erase gate.

1 8. (Once Amended) A memory array disposed on a substrate comprising a plurality of memory
2 cells each having a floating gate separated from said substrate by a first insulating layer, an erase
3 gate, a control gate separated from said floating gate by a second insulating layer, a source
4 region, and a drain region, comprising:
5 a plurality of rows and columns of interconnected memory cells wherein the control gates
6 of memory cells in the same row are connected by a common word-line, the erase gates of the
7 memory cells in the same rows are connected by a common erase line, the source regions of the
8 memory cells in the same rows are connected by a common source line, and the drain regions of
9 memory cells in the same columns are commonly connected via a common drain line, wherein at
10 least a portion of each said control gate is disposed over a portion of said substrate and separated
11 therefrom by said second insulating layer, and wherein a portion of said control gate is not
12 disposed over said floating gate; and
13 control circuit connecting to said word-lines, erase lines, source lines and drain lines for
14 operating one or more memory cells of said memory array.

1 16. (Once Amended) A semiconductor device having at least one transistor, the device
2 comprising:
3 a substrate having a channel region;
4 a first insulating layer disposed over said channel region and over at least a portion of
5 said substrate;
6 a floating gate generally disposed over said channel region and separated therefrom by
7 said first insulating layer, said floating gate having at least two side walls and a top surface;